LP5951 Evaluation Board

National Semiconductor
Application Note 1486
Klaus Scheitinger
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Introduction

This evaluation board is designed to enable independent evaluation of the LP5951 electrical performance. Each board is pre-assembled and tested in the factory.

The evaluation kits are available in two options: LP5951MF-1.8EV and LP5951MF-2.5EV. For other voltage and package options, the device can be ordered from LP5951 product folder on National's website. The board offers two different assembly options: SC70-5 package (MG) on top side (TOP) or SOT23-5 package on bottom side (BOT) of the board. Only one side will be assembled at a time.

General Description

The LP5951 converts high input voltages to lower output voltages while consuming low quiescent current. The LP5951 is capable of operating with an input voltage range from 1.8V to 5.5V for fixed output voltage options from 1.3V to 3.3V. The LP5951 can supply a maximum output current of 150mA and is particulary suitable for portable, battery-powered systems. It also features internal protection against short-circuit currents and over-temperature conditions.

The input voltage, applied between V_{IN} and GND should be at least 0.35V above the output voltage to operate the device out of dropout with a minimum of 1.8V and no higher than 5.5V. Input connections should be kept reasonably short (<30cm) to minimise input inductance and ensure optimum transient performance.

ON/OFF control of the LP5951 is provided on the evaluation board by a logic signal applied to the V_{EN} pin. To simplify the enabling of the device, a three pin jumper is provided on the board. The middle pin is directly connected to the V_{EN} pin of the device. A logic signal with a minimum of 0.9V to enable the device or with a maximum of 0.4V to disable the device can be directly connected to this jumper pin in the middle. Alternatively the middle pin can be shorted to the pin next to it to the left or to the right marked OFF or ON.

A load of 150mA maximum may be connected from the V_{OUT} pin to GND.

At the bottom of each side of the board the package (SC70-5 or SOT23-5) and the output voltage option (1.3V, 1.5V, 1.8V, 2.0V, 2.5V, 2.8V, 3.0V or 3.3V) is printed.

The V_{OUT_S} pin represents a sense path to the output voltage pin and can be used for more precise voltage measurements.

The schematic and board layout are shown below:

Schematic Diagram

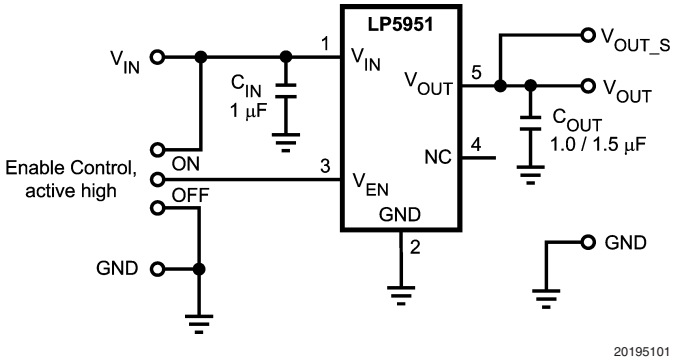

FIGURE 1: Evaluation Board Schematic

Evaluation Board Component and Pin Layout

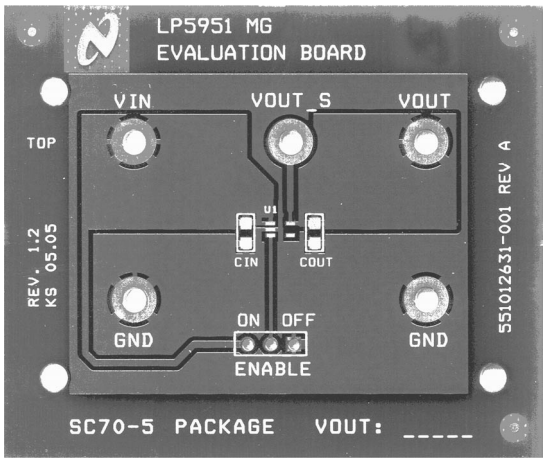

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FIGURE 2: TOP Side, SC70-5 Package (MG)
Board Size: 60mm x 50mm

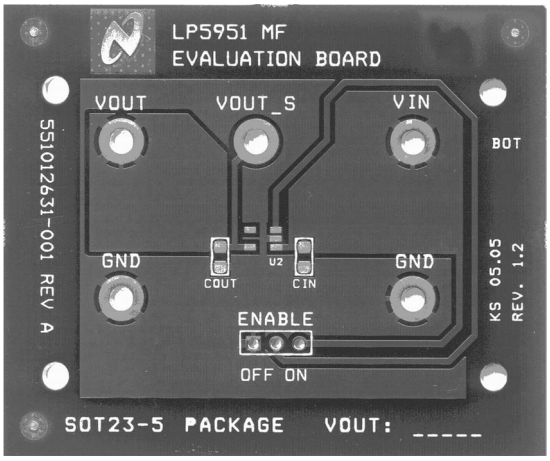

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FIGURE 3: BOTTOM Side, SOT23-5 Package (MF)

Connection Diagrams

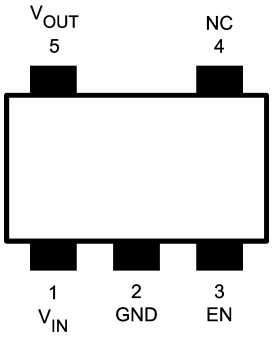

FIGURE 4: SOT23-5 (MF), Top View

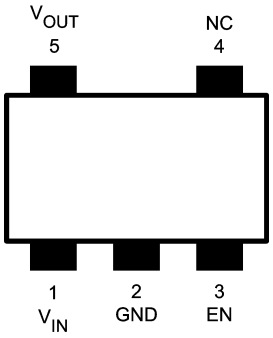

FIGURE 5: SC70-5 (MG), Top View

Pin Descriptions

Pin #	Name	Description
1	V_{IN}	Input voltage. Input range: 1.8V to 5.5V
2	GND	Ground
3	EN	Enable pin logic input: Low = shutdown, High = normal operation. This pin should not be left floating. Short to V_{IN} using attached jumper for normal operation.
4	NC	No internal connection
5	V_{OUT}	Regulated output voltage

Bill of Materials

Item	Description	Amount	Footprint	Mfg., Part Number
C_{IN}	Ceramic capacitor, 1µF, X5R	1	0603	TDK, C1608X5R1A105K
C_{OUT}	Ceramic capacitor, 1µF, X5R or Ceramic capacitor, 1.5µF, X5R	1	0603	TDK, C1608X5R1A105K (for 1.3V to 2.5V options) or TDK, C1608X5R1C155K (for 2.8V to 3.3V options)
U_1 or U_2	LP5951 LDO Regulator	1	SC70-5 or SOT23-5	National Semiconductor, LP5951MG-x.x or National Semiconductor, LP5951MF-x.x
V_{IN}, V_{OUT_S}, V_{OUT}, GND	Test pins	5		Cambion, 160-1026-02-05

Application Hints

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

The allowable power dissipation for the device in a given package can be calculated using the following equation:

$PD = (T_{J(MAX)} - T_A) / \theta_{JA}$

With a θ_{JA} = 220˚C/W, the device in the SOT23-5 package returns a value of 454mW with a maximum junction temperature of 125˚C at T_A of 25˚C. For the SC70-5 package with a θ_{JA} = 415˚C/W, the device returns a value of 241mW.

The actual power dissipation across the device can be estimated by the following equation:

$P_D \approx (V_{IN} - V_{OUT}) * I_{OUT}$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

Application Hints (Continued)

Based on these considerations the following 'Output Current Derating' can be calculated:

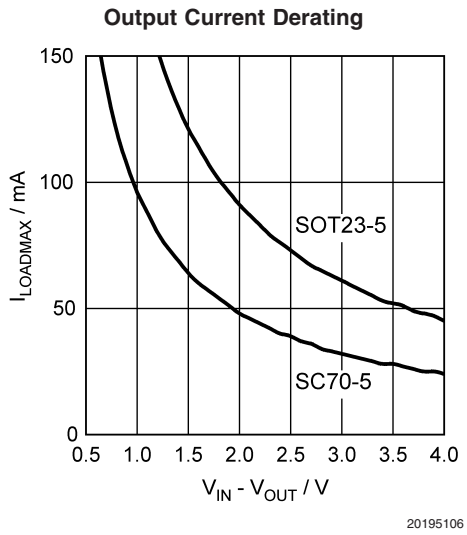

FIGURE 6: Maximum Load Current vs (V_{IN} - V_{OUT}), T_A = 85˚C, V_{OUT} = 1.5V

EXTERNAL CAPACITORS

A ceramic capacitor of 1.0µF is recommended and assembled at the input (C_{IN}) .

At the output (C_{OUT}) the following ceramic capacitors are suitable:

- V_{OUT} < 2.8V: 1.0µF
- V_{OUT} ≥ 2.8V: 1.5µF.

For further details on recommended capacitors and capacitor characteristics please see bill of materials above and the datasheet.

National Semiconductor
Americas Customer Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
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Asia Pacific Customer Support Center
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National Semiconductor
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